Amendments to the Specification:

Please replace the paragraph beginning on page17, line 25, and continuing to page 19, line 9, with the following rewritten paragraph:

When an abnormal firmware is written, the first processor 1 can not transmit the response pulse having the LOW level to the B line Lb because the firmware is not normal after activation. The second processor 2 monitors the response pulse through the port. If the second processor 2 can not detect the response pulse, it again transmits the reset signal to the A line La. This reset signal causes the first processor 1 to be again activated. However, since the first processor 1 can not transmit the response pulse to the B line Lb, the reset signal is again transmitted. When this operation is repeated five times, the second processor 2 judges that the firmware of the first processor 1 is not normal, and compulsorily resets the first processor 1 (refer to Fig. 4). The reason why the reset operation is repeated five times at this time is to avoid the processor from becoming at the compulsory reset state~~,~~ when ~~the~~ noise or the like causes the processor to carry out an erroneous operation, even if ~~the~~ normal firmware is written. If the process carries out the erroneous operation in the condition that the normal firmware is written, the process is recovered by one reset operation, and it is returned back to normal operation. In this case, the second processor 2 carries out an operation similar to that of the so-called watch dog timer. Since the first processor 1 is compulsorily reset, the ~~ASYNCE~~ ASYNC line for the transmission (TXD) connected to the first processor 1 is set at the HIGH level. Thus, the second processor 2 can normally carry out a communication. Hence, even if ~~the~~ abnormal firmware is written, the normal firmware can be again downloaded. This is similar in a case that the flash ROM is empty at an initial state. If the processor is activated when the flash ROM is empty, the firmware ~~is~~ can run away, which may have an influence on a communication line. However, since the first processor 1 is compulsorily reset, it is possible to set the downloadable state.